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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,855	02/04/2004	Marius K. Orlowski	SC13155TP	3511
23125	7590	09/06/2005	EXAMINER	
FREESCALE SEMICONDUCTOR, INC. LAW DEPARTMENT 7700 WEST PARMER LANE MD:TX32/PL02 AUSTIN, TX 78729			SMOOT, STEPHEN W	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary

Application No.

10/771,855

Applicant(s)

ORLOWSKI ET AL.

Examiner

Stephen W. Smoot

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>2-4-04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office action is in response to application papers filed on 04 February 2004.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 13-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13 recites the limitation "the second layer" in line 2. There is insufficient antecedent basis for this limitation in claim 13.

Claims 14-17 are rejected under 35 U.S.C. 112, second paragraph, because they depend on claim 13.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6, 11-13, 18-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Sugiyama et al. (US 6,369,438 B1 – from applicant's IDS).

Referring to Figs. 1A-1C, 5, column 5, line 1 to column 7, line 55, and column 9, lines 14-35, Sugiyama et al. disclose a method of forming a field effect transistor that includes the following features:

- A single crystal silicon substrate (11) is provided;
- An oxygen-containing single crystal silicon layer (12) is deposited on a top surface of the single crystal silicon substrate (11);
- The oxygen-containing single crystal silicon layer (12) has about 2 atom % oxygen;
- A single crystal SiGe layer (13) and a single crystal silicon layer (14) are then sequentially grown on the oxygen-containing single crystal silicon layer (12);
- The substrate (11) and overlying layers (12, 13, 14) are then subjected to thermal oxidation resulting in the formation of a silicon oxide layer (15) at the top surface

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of the substrate (11) and a silicon oxide layer (16) on the surface of the single crystal silicon layer (14) as shown in Fig. 1C;

- The thermal oxidation step can include water vapor at a temperature of 950 degrees C;
- Subsequently a field effect transistor can be formed over this layered structure as shown in Fig. 5; and
- The field effect transistor includes a gate electrode (32) with adjacent source/drain regions (33) formed in the SiGe layer (13a) and the silicon layer (14a), which implies that a channel region is formed in the SiGe layer (13a) and the silicon layer (14a) between the source/drain regions (33) and below the gate electrode (32).

These are all of the limitations set forth in claims 1-6, 11-13, 18-26 of the applicant's invention.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 7-10, 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugiyama et al. (US 6,369,438 B1 – from applicant's IDS) as applied to claims 6, 13 above, and further in view of Houg et al. (US 2002/0102775 A1).

As shown above, Sugiyama et al. anticipate claims 6, 13 of the applicant's invention. Also, as shown above, Sugiyama et al. disclose the further limitations as set forth in claims 8-10, 15 of the applicant's invention. However, Sugiyama et al. do not expressly teach or suggest the further limitations to claim 6 as set forth in claim 7 of the applicant's invention or the further limitations to claim 13 as set forth in claim 14 of the applicant's invention, which, for both claims 7, 14, are to remove at least a portion of the oxide layer formed on top of the silicon layer and to form a gate dielectric on the silicon layer. Houg et al. teach that native oxides should be completely removed from a silicon surface prior to forming a gate oxide layer (see abstract).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Sugiyama et al. and Houg et al. in order to completely remove the oxide layer, from the silicon layer of Sugiyama et al., prior to forming a gate oxide layer on the silicon layer, as taught by Houg et al. Houg et al. recognize that complete removal of the native oxides improves the quality of the subsequently formed gate oxide and results in increased breakdown field as well as reduced interface trap density (see abstract).

7. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugiyama et al. (US 6,369,438 B1 – from applicant's IDS) and Houg et al. (US

2002/0102775 A1) as applied to claim 15 above, and further in view of Park et al. (US 6,429,084 B1).

As shown above, the combination of Sugiyama et al. and Houngh et al. has all of the limitations as set forth in claim 15 of the applicant's invention. However, this combination lacks the further limitations as set forth in claim 16-17 of the applicant's invention, which are elevated source/drain regions (claim 16) and source/drain extensions (claim 17). Referring to column 1, line 50 to column 3, line 29, Park et al. teach a field effect transistor formed on an SOI substrate that includes elevated source/drain regions (36 in Fig. 7) and source/drain extensions (35 in Fig. 10).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to further combine the teachings of Sugiyama et al. and Houngh et al. with those of Park et al. in order to include elevated source/drain regions and source/drain extensions, as taught by Park et al. Elevated source/drain regions are recognized in the art as a way to reduce junction leakage in a field effect transistor and source/drain extensions are recognized in the art as a way to reduce hot carrier effects in the channel region of a field effect transistor.


Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SWS


STEPHEN W. SMOOT
PRIMARY EXAMINER